

What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

(a) first and second semiconductor regions formed in a semiconductor substrate;

(b) first and second conductors formed at an upper portion of said semiconductor substrate and on a portion between said first and second semiconductor regions;

(c) a first insulator film formed between said first conductor and said semiconductor substrate; and

(d) a second insulator film formed between said second conductor and said semiconductor substrate, the second insulator film having a charge accumulation portion therein, wherein

(e) while a positive potential is applied to said first conductor, holes are injected into said charge accumulation portion, in which electrons are accumulated, and thereby an erase operation is performed.

2. The nonvolatile semiconductor memory device according to claim 1,

wherein the hole injection in said (e) is performed in a state in which a current flows between said first and second semiconductor regions.

3. The nonvolatile semiconductor memory device according to claim 2,

wherein the hole injection in said (e) is performed by flowing a current having a value of 0.1 to 10  $\mu$ A between

said first and second semiconductor regions.

4. The nonvolatile semiconductor memory device according to claim 2,

wherein the hole injection in said (e) is performed by automatically controlling such a current flowing between said first and second semiconductor regions that a value thereof is made constant by using a circuit.

5. The nonvolatile semiconductor memory device according to claim 1,

wherein by erasing said (e), a threshold voltage of a MISFET using said second conductor as a gate electrode is reduced.

6. The nonvolatile semiconductor memory device according to claim 1,

wherein said first semiconductor region is disposed on a side of said first conductor and said second semiconductor region is disposed on a side of said second conductor, and

the holes in said (e) are generated by: applying a first potential to said first conductor; applying a second potential to said second conductor; and thereby accelerating, through said second potential, electrons flowing between said first and second semiconductor regions to cause an impact ionization phenomenon.

7. The nonvolatile semiconductor memory device according to claim 1,

wherein an injection position of the holes in said (e)

is near an end of said second insulator film on a side of said first conductor.

8. The nonvolatile semiconductor memory device according to claim 1,

wherein a distribution of electrons accumulated in the charge accumulation portion in said (e) has a peak near an end of a side of said first conductor.

9. The nonvolatile semiconductor memory device according to claim 1,

wherein electrons accumulated in the charge accumulation portion in said (e) are electrons injected, by applying respective different potentials to said first and second conductors, from said semiconductor substrate located under a boundary between said first and second conductors.

10. The nonvolatile semiconductor memory device according to claim 1,

wherein a potential applied to said second semiconductor region when the holes in said (e) are injected into the charge accumulation portion is equal to that applied to said second semiconductor region when the electrons in said (e) are injected into the charge accumulation portion, and

a current flowing between said first and second semiconductor regions when the holes in said (e) are injected into the charge accumulation portion is equal to that flowing between said first and second semiconductor

regions when the electrons in said (e) are injected into the charge accumulation portion.

11. The nonvolatile semiconductor memory device according to claim 1,

wherein a potential applied to said second semiconductor region when the holes in said (e) are injected into the charge accumulation portion is higher than that applied to the second semiconductor region when the electrons in said (e) are injected into the charge accumulation portion, and

a current flowing between said first and second semiconductor regions when the holes in said (e) are injected into the charge accumulation portion is equal to that flowing between said first and second semiconductor regions when the electrons in said (e) are injected into the charge accumulation portion.

12. The nonvolatile semiconductor memory device according to claim 1,

wherein a potential applied to said second semiconductor region when the holes in said (e) are injected into the charge accumulation portion is equal to that applied to said second semiconductor region when the electrons in said (e) are injected into the charge accumulation portion, and

a current flowing between said first and second semiconductor regions when the holes in said (e) is injected into the charge accumulation portion is larger

than that flowing between said first and second semiconductor regions when the electrons in said (e) are injected into the charge accumulation portion.

13. The nonvolatile semiconductor memory device according to claim 1,

wherein said charge accumulation portion is a trap insulator film formed in said second insulator film.

14. The nonvolatile semiconductor memory device according to claim 1,

wherein said charge accumulation portion is a nitride film formed in said second insulator film.

15. A nonvolatile semiconductor memory device according to claim 1,

wherein said second insulator film is a laminating film of a first oxide film, a nitride film, and a second oxide film.

16. The nonvolatile semiconductor memory device according to claim 15,

wherein said first and second oxide films each have a thickness of 3 nm or more.

17. The nonvolatile semiconductor memory device according to claim 1,

wherein said charge accumulation portion is constituted by a plurality of conductive fine particles formed in said second insulator film.

18. The nonvolatile semiconductor memory device according to claim 1, wherein:

(f) a third semiconductor region is formed in said semiconductor substrate disposed under said second conductor;

(f1) a conductivity type of an impurity constituting said third semiconductor region is the same as that of an impurity constituting said second semiconductor region disposed on a side of said second conductor; and

(f2) an impurity concentration of said third semiconductor region is lower than that of said second semiconductor region.

19. The nonvolatile semiconductor memory device according to claim 1,

wherein the erase operation in said (e) is performed while another potential is applied to said second semiconductor region disposed on a side of said second conductor, and

a depletion layer extending from said second semiconductor region extends to said semiconductor substrate disposed under a boundary between said first and second conductors.

20. The nonvolatile semiconductor memory device according to claim 1,

wherein, when no charge is accumulated in said charge accumulation portion, a threshold value of a MISFET using said second conductor as a gate electrode is negative and is smaller than that of a MISFET using said first conductor as a gate electrode.

21. A nonvolatile semiconductor memory device comprising:

(a) first and second semiconductor regions formed in a semiconductor substrate;

(b) first and second conductors formed at an upper portion of said semiconductor substrate and on a portion between said first and second semiconductor regions;

(c) a first insulator film formed between said first conductor and said semiconductor substrate; and

(d) a second insulator film formed between said second conductor and said semiconductor substrate, the second insulator film having a charge accumulation portion therein, wherein

(e) while a current flows between said first and second semiconductor regions, holes are injected into said charge accumulation portion, in which electrons are accumulated, and thereby an erase operation is performed.

22. A nonvolatile semiconductor memory device comprising:

(a) first and second semiconductor regions formed in a semiconductor substrate;

(b) first and second conductors formed at an upper portion of said semiconductor substrate and on a portion between said first and second semiconductor regions;

(c) a first insulator film formed between said first conductor and said semiconductor substrate; and

(d) a second insulator film formed between said

second conductor and said semiconductor substrate, the second insulator film having a charge accumulation portion therein, wherein

(e) while different potentials are respectively applied to said first and second conductors, electrons flowing between said first and second semiconductor regions are accumulated near an end of said second insulator film on a side of said first conductor and thereby a write operation is performed, and

(f) while a positive potential is applied to said first conductor, holes generated between said first and second semiconductor regions are injected into a portion, which is disposed near the end of said second insulator film and on a side of said first conductor, and thereby an erase operation is performed.

23. A nonvolatile semiconductor memory device comprising: a plurality of memory cells disposed in an array manner, each of the memory cells including:

(a) first and second semiconductor regions formed in a semiconductor substrate;

(b) first and second conductors formed at an upper portion of said semiconductor substrate and on a portion between said first and second semiconductor regions;

(c) a first insulator film formed between said first conductor and said semiconductor substrate; and

(d) a second insulator film formed between said second conductor and said semiconductor substrate, the

second insulator film having a charge accumulation portion therein, wherein

(e) the memory device including: a plurality of first lines for connecting said first conductors of the memory cells arranged in a first direction in said plurality of memory cells; and a plurality of second lines for connecting said first semiconductor regions disposed on a side of said first conductor in the memory cells arranged in a second direction perpendicular to said first direction, and

(f) while a positive potential is applied to said first line connected with a selected memory cell of said plurality of memory cells, holes are injected into said charge accumulation portion of said selected memory cell, in which electrons are accumulated, and thereby an erase operation is performed.

24. The nonvolatile semiconductor memory device according to claim 23,

wherein the holes in said (f) are generated by: applying potentials to said first lines connected with said selected memory cell and to said second semiconductor region of said selected memory cell; and accelerating, through the potential applied to said second semiconductor region, electrons flowing between said first and second semiconductor regions of said selected memory cell to cause an impact ionization phenomenon.

25. The nonvolatile semiconductor memory device

according to claim 23,

wherein an injection position of the holes in said (f) is near an end of said second insulator film in said selected memory cell and on a side of said first conductor.

26. The nonvolatile semiconductor memory device according to claim 23,

wherein the electrons accumulated in the charge accumulation portion in said (f) are electrons which are injected from said semiconductor substrate disposed under a boundary between said first and second conductors by applying respective different potentials to said first and second conductors of said selected memory cell.

27. The nonvolatile semiconductor memory device according to claim 23,

wherein the erase operation in said (f) is performed per single unit of said selected memory cell, in which:

(f1) the erase operation is performed while a first potential is applied to said first line connected with said selected memory cell and when a second potential lower than said first potential is applied to said second line connected with said selected memory cell; and

(f2) the erase operation is prohibited by applying a third potential equal to or higher than said first potential to said second line connected with another memory cell connected with said first line connected with said selected memory cell.

28. The nonvolatile semiconductor memory device

according to claim 23,

wherein the erase operation in said (f) is performed per group of said memory cells arranged in said first direction by:

(f1) applying a first potential to a single first line of said plurality of first lines, and

(f2) applying a second potential lower than said first potential to said plurality of second lines.

29. The nonvolatile semiconductor memory device according to claim 23,

wherein the erase operation in said (f) is performed per block of  $n \times m$  ones of said memory cells by:

(f1) applying a first potential to  $n$  first lines of said plurality of first lines, and

(f2) applying a second potential lower than said first potential to  $m$  second lines of said plurality of second lines.

30. The nonvolatile semiconductor memory device according to claim 23,

wherein the erase operation in said (f) is performed by:

(f1) applying a first potential ( $V_1$ ) to the first line which is connected with said selected memory cell in said plurality of first lines,

(f2) applying a second potential ( $V_2$ ) to the first line which is not connected with said selected memory cell in said plurality of first lines,

(f3) applying a third potential (V3) to the second line which is connected with said selected memory cell in said plurality of second lines, and

(f4) applying a fourth potential (V4) to the second line which is not connected with said selected memory cell in said plurality of second lines,

in which

(f5) said first to fourth potentials meet the following conditions:

said third potential is lower than said first potential ( $V3 < V1$ ) and is equal to or higher than said second potential ( $V3 \geq V2$ ); and

said fourth potential is equal to or higher than said first potential ( $V4 \geq V1$ ) and is equal to or higher than said second potential ( $V4 \geq V2$ ).

31. A nonvolatile semiconductor memory device according to claim 23, further comprising:

(g) a plurality of third lines for connecting said second semiconductor regions of the memory cells arranged in said first direction in said plurality of memory cells, wherein said plurality of third lines are connected with one another in a predetermined unit.

32. The nonvolatile semiconductor memory device according to claim 23, further comprising:

(g) a plurality of third lines for connecting said second conductors of the memory cells arranged in said first direction in said plurality of memory cells,

wherein said plurality of third lines are connected with one another in a predetermined unit.

33. A nonvolatile semiconductor memory device comprising: a plurality of memory cells arranged in an array manner, each of the memory cells including:

(a) first and second semiconductor regions formed in a semiconductor substrate;

(b) first and second conductors formed at an upper portion of said semiconductor substrate and on a portion between said first and second semiconductor regions;

(c) a first insulator film formed between said first conductor and said semiconductor substrate; and

(d) a second insulator film formed between said second conductor and said semiconductor substrate, the second insulator film having a charge accumulation portion therein,

wherein

(e) the memory device includes: a plurality of first lines for connecting said first conductors of the memory cells arranged in a first direction in said plurality of memory cells; a plurality of second lines for connecting said second semiconductor regions located on sides of said second conductors in said memory cells arranged in a second direction perpendicular to said first direction; and a plurality of third lines for connecting said first semiconductor regions of said memory cells arranged in said first direction, and

(f) while a positive potential is applied to said first line connected with a selected memory cell in said plurality of memory cells, holes are injected into said charge accumulation portion of said selected memory cell, in which electrons are accumulated, and thereby an erase operation is performed.

34. The nonvolatile semiconductor memory device according to claim 33,

wherein the holes in said (f) are formed by: applying potentials to said first and second lines connected with said selected memory cell; and accelerating electrons flowing between said first and second semiconductor regions of said selected memory cell by the potential applied to said second semiconductor region in said selected memory cell to cause an impact ionization phenomenon.

35. The nonvolatile semiconductor memory device according to claim 33,

wherein an injection position of the holes in said (f) is near an end of said second insulator film in the selected memory cell and on a side of said first conductor.

36. The nonvolatile semiconductor memory device according to claim 33,

wherein the electrons accumulated in the charge accumulation portion in said (f) are electrons which are injected from said semiconductor substrate disposed under a boundary between said first and second conductors by applying respective different potentials to said first and

second conductors of said selected memory cell.

37. The nonvolatile semiconductor memory device according to claim 33,

wherein the erase operation in said (f) is performed per single unit of said memory cell, in which:

(f1) the erase operation is performed while a first potential is applied to said first line connected with said selected memory cell and a second potential higher than a third potential, which is applied to said third line connected with said selected memory cell, is applied to said second line connected with said selected memory cell; and,

(f2) the erase operation is prohibit by applying a fourth potential equal to or lower than said third potential, to said second line connected with another memory cell connected with said first line connected with said selected memory cell.

38. The nonvolatile semiconductor memory device according to claim 33,

wherein the erase operation is said (f) is performed per group of said memory cells arranged in said first direction by:

(f1) applying a first potential to a single first line of said plurality of first lines;

(f2) applying a second potential to each of said plurality of second lines; and

(f3) applying a third potential lower than said

second potential, to said third line of said memory cell connected with said single first line.

39. The nonvolatile semiconductor memory device according to claim 33,

wherein the erase operation in said (f) is performed per block of  $n \times m$  ones of said memory cells by:

(f1) applying a first potential to each of  $n$  first lines of said plurality of first lines;

(f2) applying a second potential to each of  $m$  second lines of said plurality of second lines; and

(f3) applying a third potential lower than said second potential to each of  $n$  third lines corresponding to said  $n$  first lines.

40. The nonvolatile semiconductor memory device according to claim 33,

wherein the erase operation in said (f) is performed by:

(f1) applying a first potential ( $V_1$ ) to the first line, which is connected with said selected memory cell in said plurality of first lines;

(f2) applying a second potential ( $V_2$ ) to the first line, which is not connected with said selected memory cell in said plurality of first lines;

(f3) applying a third potential ( $V_3$ ) to the third line, which is connected to said selected memory cell in said plurality of third lines; and

(f4) applying a fourth potential ( $V_4$ ) to the third

line, which is not connected with said selected memory cell in said plurality of third lines,

in which

(f5) said first to fourth potentials meet the following conditions:

said third potential is lower than said first potential ( $V3 < V1$ ) and is equal to or higher than said second potential ( $V3 \geq V2$ ); and

said fourth potential is equal to or higher than said first potential ( $V4 \geq V1$ ) and is equal to or higher than said second potential ( $V4 \geq V2$ ).

41. The nonvolatile semiconductor memory device according to claim 33,

wherein said plurality of third lines are connected with one another in a predetermined unit.

42. The nonvolatile semiconductor memory device according to claim 33, further comprising:

(g) a plurality of fourth lines for connecting said second conductors of the memory cells arranged in said first direction in said plurality of memory cells,

wherein said plurality of fourth lines are connected with one another in a predetermined unit.